A Fully Passivated Ultra Low Noise W-Band Monolithic InGaAs/InAlAs/InP HEMT Amplifier

G. I. Ng, R. Lai, Y. Hwang, H. Wang, D. C. W. Lo, T. Block, K. Tan,
D. C. Streit, R. M. Dia, A. Freudenthal, P. D. Chow and J. Berenz

TRW Electronic Systems and Technology Division
One Space Park
Redondo Beach, CA 90278
Tel: (310) 814 1727, Fax: (310) 814 4448

ABSTRACT

A W-band 3-stage monolithic low noise amplifier has been developed based on InGaAs/InAlAs/InP HEMT MMIC technology. Both wafer passivation and stabilization bakes have been introduced for the first time to the MMIC process to make it more suitable for production. A minimum noise figure of 3.3 dB and 20 dB associated gain has been achieved at 94 GHz and represents the best reported performance to date for any passivated multi-stage MMIC LNA's operating at W-band.

INTRODUCTION

W-band low noise amplifiers represent a key component in several advanced systems for space and military applications such as radiometry, communication, mmW imaging and smart munitions and commercial applications such as automotive radar. InGaAs/InAlAs/InP High Electron Mobility Transistor Monolithic Millimeter-Wave Integrated Circuit (InP HEMT MMIC) technology has been promising at W-band based on the very low noise figures achieved at a discrete device level [1-2]. On the MMIC level, the best reported data at W-band for monolithic InP HEMT multi-stage MMIC LNA has been an unpassivated three stage LNA with 4.3 dB noise figure and 19 dB gain at 100 GHz [3]. However, to simultaneously achieve high performance, reliability and lower cost, the InP HEMT MMIC process must be made suitable for production by introducing device passivation and wafer level stabilization bakes. In this work, we present for the first time a fully passivated monolithic low noise 3-stage single ended W-band InP HEMT amplifier with a minimum noise figure of 3.3 dB with 20 dB associated gain at 94 GHz and less than 20 mW total dissipated d.c. power. The results were achieved with a silicon nitride passivated 0.1 μm gate length InP HEMT MMIC process which is suitable for production. The performance is a significant improvement over our first iteration W-band design [3], and represents the best noise performance reported to date for any passivated multi-stage MMIC LNA operating at this frequency band [4,5].

Passivation and Stability-Bake Experiments

To develop a more robust InP HEMT MMIC process, two important process steps have been introduced: a 500Å PECVD silicon nitride (SiN) passivation process and a wafer level 200°C stabilization bake step. For 0.1μm gate-length InP HEMTs measured at V_{ds}=1V, the 500Å SiN passivation layer on InP HEMTs does not affect the device performance appreciably. The average G_{mp} value only decreases by 1.6%. and is comparable to the previously reported

95CH3577-7/95/0000-0063$01.00 © 1995 IEEE

results for ECR silicon nitride passivated InP HEMTs [6]. The rf performance of these devices also show only a small change with f_T decreases by 3.9% and f_{max} decreases by 8.2%. The small decreases in f_T and f_{max} are mainly attributed to small changes observed in C_{gd} and C_{ds} (<10%).

After SiN passivation, a wafer level stabilization bake is added to improve the stability, robustness and reliability of the MMICs and can provide a screen for very weak MMIC parts. We have conducted a step-stress test starting at 200°C bake temperature and increasing the temperature in pre-determined time intervals and measuring device d.c. and rf parameters (G_{mp}, Imax, f_T and f_{max}) at each interval. Table 1 shows the percentage change in the device parameters after 200°C, 215°C and 230°C baking for 72 hrs, 48 hrs and 48 hrs respectively. The changes are calculated with respect to the device parameters obtained after SiN passivation. As seen in Table 1, both dc and rf parameters show minimal change up to 230°C bake temperature and no sudden or catastrophic degradations were observed. Based on this data, a 200°C stabilitization bake has been implemented into our InP HEMT MMIC process.

Circuit Fabrication, Design and Performance

The layer structure for the InP HEMT is similar to the design used in the first iteration [3] which employs a pseudomorphic 60% Indium InGaAs channel. The devices used have 0.1μm gate-length and the circuit fabrication steps are similar to those reported in [3] except in this work the SiN passivation and stabilization bake steps are added. Typical transconductances greater than 800 mS/mm and f_T's greater than 160 GHz were obtained on the passivated InP HEMTs after 200°C stabilization bake. After SiN passivation and 200°C sta-bake, the G_{mp} and f_T for the monitored discrete devices only change by -2.3% and -3.5% respectively. These results once again show minimal change in the device performance after passivation and sta-bake steps.

The circuit design of the single-ended 3-stage W-band LNA employs a 4 finger 40 μm InP HEMT for each stage. The design methodology is similar to the previously published W-band monolithic LNAs [7]. A wet chemical etch is used to form backside via holes through the InP substrate for grounding. The photograph of the completed chip is shown in Fig. 1 and the overall chip size is 2.5mm x 1.2mm.

The W-band monolithic amplifier was measured using a verified W-band on-wafer probe test set [8]. Measured results of other W-band LNA chips from the on-wafer test set have been observed to close to the in-fixture test results, which provided a validation of the on-wafer probing system. The LNA exhibited a minimum noise figure of 3.3 dB at 94 GHz with 20 dB associated gain and less than 4.4 dB noise figure between 92-96 GHz (Fig. 2). The total LNA d.c. power dissipation was about 21 mW (V_d = 0.9V, I_d = 23.8 mA) which is typically two to three times less than GaAs HEMT LNAs versions. When biased for higher gain, the amplifier exhibited 22.1 dB gain at 93 GHz (7.4 dB gain per stage) with 3.7 dB noise figure (Fig. 3). These results are the best ever reported for any passivated HEMT W-band MMIC LNA and is the first reported InP HEMT LNA at W-band with passivation. We attribute the excellent performance to the improved second iteration design based on a more mature process which is suitable for production.

Summary

We have studied the impact of silicon nitride passivation and stabilization bake on 0.1μm InGaAs/InAlAs/InP HEMTs. Our results indicate that these additional steps show minimal change in the device dc and rf performance. It can therefore be

incorporated in our InP HEMT MMIC process and are suitable for production. Using this technology, we have developed a fully passivated W-band 3-stage monolithic low noise amplifier with a minimum noise figure of 3.3 dB and 20 dB associated gain at 94 GHz. This, to our knowledge, is the first report of a fully passivated W-band InP HEMT MMIC LNA and has the best noise performance todate for any passivated multi-stage MMIC LNA operating W-band.

ACKNOWLEDGEMENT

The authors would like to thank Drs. B. R. Allen, E. Rezek and H. C. Yen for their helpful discussions and suggestions. Dr. P. H. Liu for his help in submicron lithography; Y. Y. Tu, N. Nguyen and J. Huang for backside processing; and S. Esparza for the W-band noise measurement.

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Temperature (°C)	Time (hours)	ΔGmp	ΔImax	ΔfT	Δfmax
200	72	1.67%	-5.15%	0.40%	1.03%
215	48	0.96%	-5.45%	0.10%	0.91%
230	48	-4.23%	-10.98%	-3.82%	0.11%

Table. 1 Changes in InP HEMT device parameters after each temperature step stress. Measurements are taken at V_{ds}=1V.

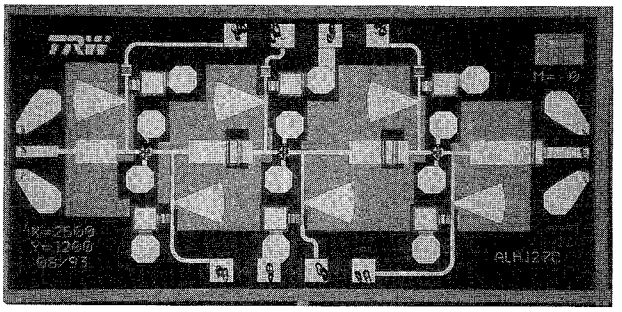

Fig. 1 Picture of the fully passivated monolithic three-stage W-band InP HEMT MMIC LNA.

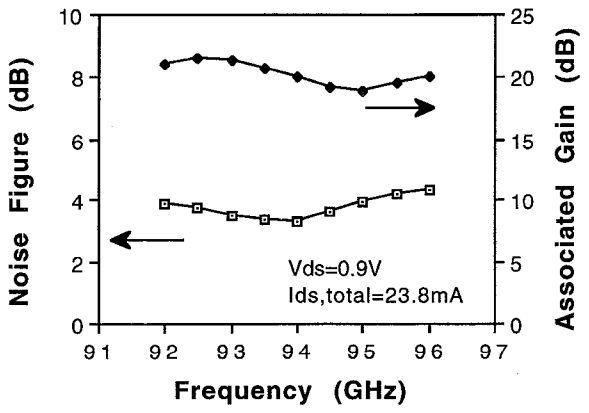

Fig. 2 Noise and gain performance of the three-stage InP HEMT MMIC LNA biased for low noise figure (V_{ds}= 0.9V, $I_{ds,total}$ = 23.8mA)

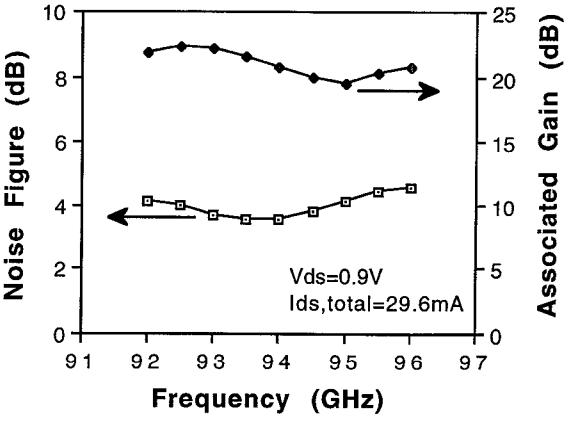

Fig. 3 Noise and gain performance of the three-stage InP HEMT MMIC LNA biased for high gain (V_{ds}= 0.9V, $I_{ds,total}$ = 29.6mA).